

4th International Workshop on
Energy Efficient SuperComputing (E2SC)
November 14th, 2016
Held in conjunction with SC'16, Salt Lake City, Utah, USA
November 13th-18th 2016

Call For Papers

Description

We will be ushering in an era with power and energy consumption as the primary concerns for scalable computing in the exascale era and beyond. To achieve viable high performance, revolutionary methods are required with a stronger integration among hardware features, system software and applications. Equally important are the capabilities for fine-grained spatial and temporal measurement and control to facilitate energy efficient computing across all layers. Current approaches for energy efficient computing rely heavily on power efficient hardware in isolation. However, it is pivotal for hardware to expose mechanisms for energy efficiency to optimize power and energy consumption for various workloads and to reduce data motion, a major component of energy use. At the same time, high fidelity measurement techniques, typically ignored in data-center level measurement, are of high importance for scalable and energy efficient inter-play in different layers of application, system software and hardware.

This workshop seeks to address important energy efficiency aspects in the HPC community that has not been previously addressed in the data center or cloud computing communities. Emphasis is given to the applications view related to significant energy efficiency improvements and to the required hardware/software stack that must include necessary power and performance measurement and analysis harnesses.

Current tools are often limited by hardware capabilities and their lack of information about the characteristics of a given workload/application. In the same manner, hardware techniques, like dynamic voltage frequency scaling, are often limited by their granularity (very coarse power management) or by their scope (a very limited system view). More rapid realization of energy savings will require significant increases in measurement resolution and optimization techniques. Moreover, the interplay between performance, power and reliability add another layer of complexity to this already difficult group of challenges.

Workshop Focus

We encourage submissions in the following areas:

- Tools for analyzing power and energy with different granularities and scope from hardware (e.g. component, core, node, rack, system) or software views (e.g. threads, tasks, processes, etc) or both.
- Techniques that enable power and energy optimizations at different

scale levels for HPC systems.

- Integration of power aware techniques in applications and throughout the software stack of HPC systems.
- Characterization of current state-of-the-art HPC system and applications in terms of Power.
- Disruptive hardware or infrastructure technologies for energy-efficient supercomputing
- Analysis of future technologies that will provide improved energy consumption and management on future HPC systems.
- Tools and techniques for exploring trade-offs between energy efficiency and resilience.

Organizing Committee

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Nick Wright	Lawrence Berkeley National Lab, USA

Important Dates

Paper Submission	2nd September 2016
Paper Notification	23rd September 2016
Final Papers Due	3rd October 2016
Conference Date	14th November 2016

Submission Guidelines

Papers should not exceed eight single-space pages (including figures, tables and references) using a 10-point on 8.5x11-inch pages. Submissions will be judged on correctness, originality, technical strength, significance, presentation quality and appropriateness. Submitted papers should not have appeared in or under consideration for another venue. A full peer-review processes will be followed with each paper being reviewed by at least 3 members of the program committee. Submissions will be made through EasyChair (<https://easychair.org/conferences/?conf=e2sc>)