The Potential Impact of Silicon Photonics Networks for Graph Analytics

PACIFIC NORTHWEST NATIONAL LABORATORY

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Talk Outline

- Workload-specific modeling at PNNL
  - Exploration of architectural concepts, from a workload perspective
  - Analytically modeling multiple metrics of interest

- Introduction to Silicon Photonics architectures
  - IBM TOPS architecture
  - Oracle Macrochip architecture

- Workloads of interest: graph analytics
  - Community Detection
  - Half-approximate Weighted Matching

- Performance analysis

- Power/energy analysis
Modeling at PNNL

► Analysis of large-scale application performance
  ■ Analytical modeling approach
  ■ Workload-centric focus
  ■ Full-scale production-level codes from a variety of domains
  ■ Current and future systems

► Interests from technologies to system architectures
  ■ Both current and future technologies
    ● Processing
    ● Memories
    ● Interconnection networks
  ■ Exploring beyond large-scale systems (e.g., embedded)

► Multiple metrics of interest
  ■ Interplay between performance, power consumption, thermal effects, and resilience
Question: what will be the impact of silicon-photonics networking technology on graph-based workloads in the 4 to 6 year timeframe?

Methodology:

- Work with architects to understand representative silicon-photonics enabled architectures of interest to DARPA’s POEM program
- Draw workloads from PNNL’s experience with graph-based applications
- Model intra-node and inter-node data movement and compare silicon-photonics enabled architectures with potential future electrical solutions
- Modeling to explore both performance and power/energy consumption

Thanks to the IBM TOPS architecture team and the Oracle Macronode architecture team for their valuable contributions
Silicon Photonics: IBM TOPS

Node architecture
- 4 sockets (64 total cores)
- Optical Hub Chip

Inter-node network
- 64 node system
- Each optical switch plane is 64×64 crossbar
- One fiber from each node to each optical switch plane
  - 16 wavelengths per fiber
  - 2.5 GB/s BW per wavelength
- 256 switch planes: 4 switch planes between each node pair with no switching

Silicon Photonics: the Oracle Macrochip

- **Macrochip architecture**
  - 64 compute/memory sites
  - Fully connected network

- **Intra-node network**
  - 128 GB/s total BW per site
  - 2 GB/s (i.e., one color) per site pair

- **Inter-node network**
  - Two sites connect to each I/O port
  - 32 ports per Macrochip create a fully-connected 32-node system
  - 256 GB/s per Macrochip pair

## Architectural Comparison Points

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<td>32</td>
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<tr>
<td>Sockets per Node</td>
<td></td>
<td>4</td>
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<td>64</td>
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<tr>
<td>Intra-Node Topology</td>
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<td>Fully-Connected</td>
<td>2D Mesh QPI</td>
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<td>Fully-Connected</td>
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<td>2D Mesh QPI</td>
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<tr>
<td>Inter-Node Topology</td>
<td></td>
<td>256 Switch Planes</td>
<td>Fat-Tree</td>
<td>Multiplane Fat-Tree</td>
<td>Fully-Connected</td>
<td>Fat-Tree</td>
<td>Multiplane Fat-Tree</td>
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<tr>
<td>Comm. Lanes (Intra/Inter)</td>
<td>16/64</td>
<td>18/4</td>
<td>18/20</td>
<td>1/128</td>
<td>18/4</td>
<td>18/48</td>
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<td>Latency (Intra/Inter) (μs)</td>
<td>0.5/0.5</td>
<td>0.5/0.5</td>
<td>0.5/0.5</td>
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<tr>
<td>Per-Lane BW (Intra/Inter) (GB/s)</td>
<td>2.5/2.5</td>
<td>1.4/6.2</td>
<td>1.4/6.2</td>
<td>2.0/2.0</td>
<td>1.4/6.2</td>
<td>1.4/6.2</td>
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- Optical networks are Silicon Photonics enabled as described in the literature
- Electrical networks are based on project 4×HDR IB technology
  - “Fixed Footprint” connects nodes with single switch (32 or 64 ports)
  - “Fixed Power” attempts to equate optical and electrical network power consumption by utilizing multiple electrical switch “planes”
Two Graph Analytics Workloads

Community Detection
- Input: Graph with weighted edges
- Output: Disjoint sets of related vertices
- Aggregated personalized all-to-all to send each edge’s target info (~1 GB)
- Iterate until $\Delta$-modularity < threshold
  - Each vertex initially its own community
  - For each vertex, determine whether modularity increases by moving to neighboring community

Large, aggregated messages
- Improve network performance
- Combine reqs with same target vertex

More computation
- Denser graph; aggregation cost
- Modularity requires collectives

Half-Approximate Weighted Matching
- Input: 2D mesh with weighted edges
- Output: Maximal weighted matching
- Two phases b/c of multi-step protocol
  - Based on locally dominant neighbor
- Phase 1:
  - Try matching each vertex
  - Aggregate messages between nodes
- Phase 2:
  - Try matching on “matched frontier”
  - Iterate until all vertices are matched
  - Use very small (24 B) messages

Small messages

Scale-40 distributed graphs

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Increasing thread count places greater relative emphasis on communication performance.

Communication performance improvement due to:
- Improved link bandwidth (40 GB/s vs. 25 GB/s)
- Message *striping* across multiple switch planes
- Greater communication concurrency due to topology
Performance Analysis: Matching

- Matching Phase 1 uses large messages in a 2D mesh pattern
  - Each site uses only four of the available 64 outgoing links
- Direct routing between Macronodes requires three hops
  - Intra-node site-to-site links offer only single-way concurrency and relatively low bandwidth
- *Indirect Intra-node Routing* may alleviate this problem by utilizing all available intra-node bandwidth
Modeled Energy Analysis

<table>
<thead>
<tr>
<th>HDR InfiniBand</th>
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<tbody>
<tr>
<td>Switch Power</td>
<td>200 Watts</td>
<td></td>
</tr>
<tr>
<td>HCA Power</td>
<td>15 Watts</td>
<td></td>
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<tr>
<td>Total Power (64)</td>
<td>1160 W</td>
<td>680 W (32)</td>
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<thead>
<tr>
<th>IBM TOPS</th>
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<tbody>
<tr>
<td>Switch Plane Power</td>
<td>20 Watts</td>
<td></td>
</tr>
<tr>
<td>Hub Chip Power</td>
<td>15 Watts</td>
<td></td>
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<tr>
<td>Total Power</td>
<td>6080 Watts</td>
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<th>Oracle Macrochip</th>
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<tr>
<td>Intra-node Network Power per Node</td>
<td>65 Watts</td>
<td></td>
</tr>
<tr>
<td>I/O Port Power per Node</td>
<td>197 Watts</td>
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<tr>
<td>Total Power</td>
<td>8384 Watts</td>
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- Fixed-footprint electrical power consumption is lower than either optical network: ~5× (IBM TOPS) & ~12× (Oracle Macrochip)
- Improved optical network performance often results in energy win
  - Exception: Lack of intra-node BW and network concurrency impairs Half-Approximate Weighted Matching performance on Oracle Macrochip
- *Fixed power* electrical networks improve performance at the cost of increased power, yielding nearly constant *energy*
Models allow us to explore *hypothetical* system configurations
- We vary the number of optical switch planes and Macrochip count
- Results are relative to the default system configuration

Results are for communication only; energy analysis does not consider core power
Conclusions

- Silicon-photonics shows promise in both performance and energy
- Silicon-photonics enabled networks show promise for graph analytics applications
  - Improved link bandwidth benefits large messages
  - Link *concurrency* benefits large numbers of small messages
  - Rich topologies benefit applications with all-to-all communication patterns
  - Performance/Energy improvements are workload dependent
- Mapping from application to architecture impacts performance
  - Algorithms with similarly rich communication patterns can find substantial performance and energy benefits
  - Algorithms whose communication patterns do not exploit topology may suffer without mechanisms such as *indirect routing*