Lies, Damn Lies and Benchmarks:

Tools vs. Methodologies

Yatin Trivedi
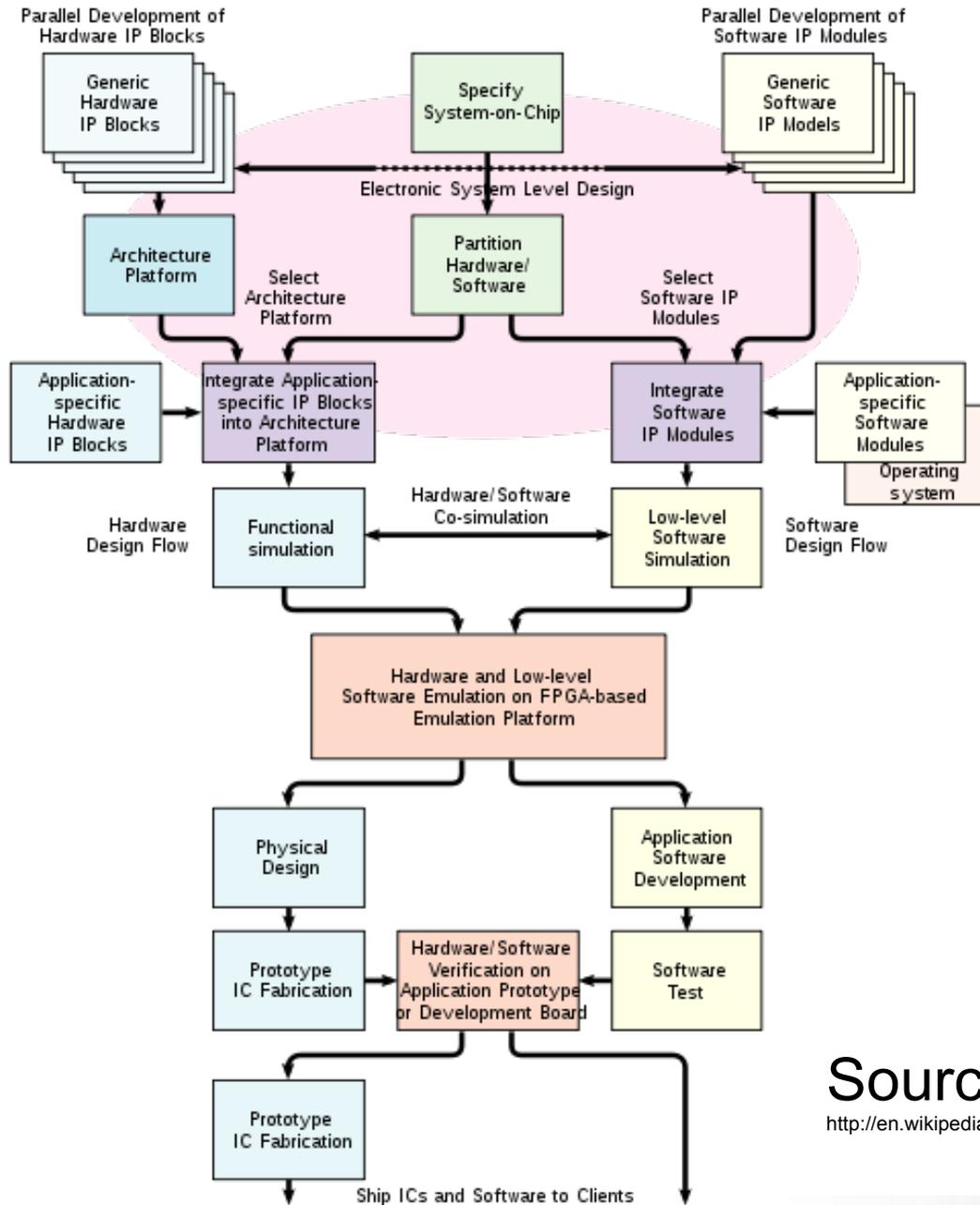
Director, Standards and Interoperability

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Grand Prix F-1 or Dunes Buggy?

SEAK Workshop, DAC 2014

A Generic Design Flow ...

Parallel Development of Hardware IP Blocks

Generic Hardware IP Blocks

Specify System-on-Chip

Parallel Development of Software IP Modules

Generic Software IP Models

Electronic System Level Design

Architecture Platform

Select Architecture Platform

Partition Hardware/ Software

Select Software IP Modules

Application-specific Hardware IP Blocks

Integrate Application-specific IP Blocks into Architecture Platform

Integrate Software IP Modules

Application-specific Software Modules

Operating system

Hardware Design Flow

Functional simulation

Hardware/Software Co-simulation

Low-level Software Simulation

Software Design Flow

Hardware and Low-level Software Emulation on FPGA-based Emulation Platform

Physical Design

Application Software Development

Prototype IC Fabrication

Hardware/Software Verification on Application Prototype or Development Board

Software Test

Prototype IC Fabrication

Ship ICs and Software to Clients

Source: Wikipedia
http://en.wikipedia.org/wiki/File:SoCDesignFlow.svg

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Grand Prix F-1 or Dunes Buggy?

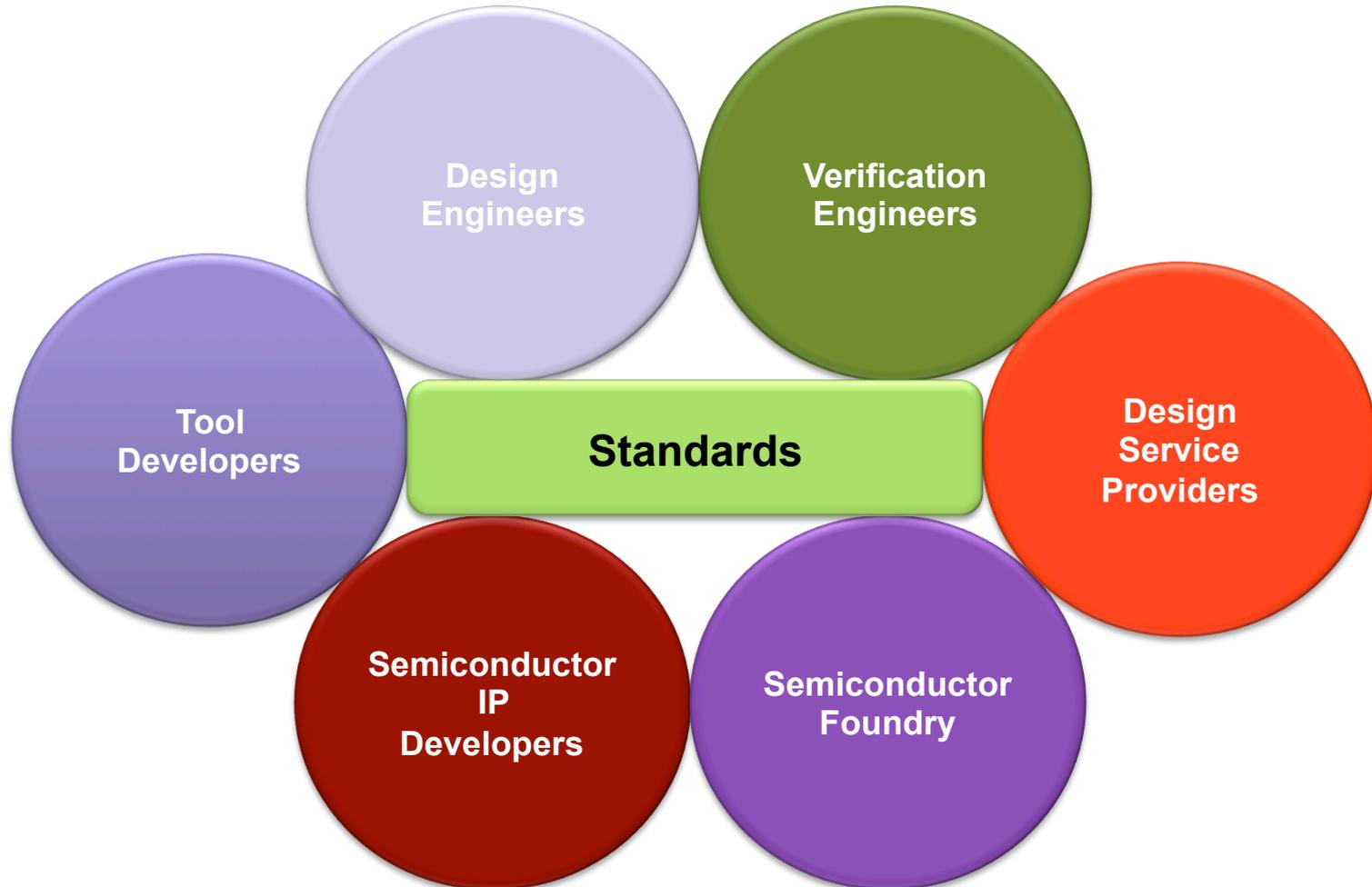**SYNOPSYS®** Accelerating Innovation

More than Meets Your Eyes

- Tools address one block at a time in your flow
  - Cost of breaking down design vs running it "flat"
- Getting design data in and out of the tool is important
  - Compliance with standards, compatibility of tools
- IP blocks come in many shapes and sizes
  - Challenge is to integrate them and validate their integration
- Standard Benchmarks vs Application Workload
  - Solution to your problem or someone else's?

- It's the Methodology, Stupid!
  - Amdahl's Law: Weakest Link controls productivity

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EDA Community and Standards

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Thank You

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