

How (Not To) Program a Computational Kernel



T. M. Low, Q. Guo, F. Franchetti: **Optimizing Space Time Adaptive Processing Through Accelerating Memory-Bounded Operations.** IEEE High Performance Extreme Computing Conference (HPEC), 2015.

But: Libraries Impose Incompatible Constraints

FFTW: contiguous rows/columns







30% gain from MPI-aware FFTW

G. Almási, B. Dalton, L. L. Hu, F. Franchetti, Y. Liu, A. Sidelnik, T. Spelce, I. G. Tānase, E. Tiotto, Y. Voronenko, X. Xue: 2010 IBM HPC Challenge Class II Submission. Winner of the 2010 HPC Challenge Class II Award (Most Productive System).



Using Libraries—Isn't that best HPC practice?

In theory, yes. But

Sometimes looks like overkill Add a whole library for a one-page function?!

People often do not use them dependencies, don't know them, "not invented here"

- Need to combine many libraries MPI, FFTW, LAPACK, Boost, STL,...
- Uneven performance and coverage across functions

not whole FFTW interface well-supported by MKL, ESSL,...



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Idea 1: Standard HPC Libraries as Kernel DSL

DSL definition and syntax

- API of standard HPC libraries
 FFTW, LAPACK, BLAS, SparseBLAS, GraphBLAS
- Libraries and language extensions for parallelism OpenMP, MPI, OpenACC
- Subset of C/C++

Single threaded, side-effect free, only standard C library calls

DSL semantics and user knowledge

- C semantics + library semantics
 Program can be executed
- Use OpenMP/OpenACC annotations to communicate meta-information #pragma omp for private(...) shared(...)

Idea 2: Interpret Program as Specification

- Make a subset of "C+OpenMP+MKL" a DSL with DSL compiler Combines code synthesis, telescoping languages, and HPC best practices
- Treat DSL program as specification, not as program computational kernels only, thus moderate code complexity
- Library calls are a DSL instructions, C fragments are "call-backs" overcomes the usual problem of code between library calls
- Establish side effect-freeness and parallelization opportunities use OpenMP/OpenACC to express independent loops, variable visibility,...
- Enables whole program optimization in domain specific compiler data layout transformations, kernel merging, target novel accelerators,...

Result: Performance Portability

- Same source code, good performance across architectures Intel Haswell, Intel Xeon PHI and Near Memory Accelerator
- Parallel cross-kernel optimized library-based code is fast 40x speed-up over C baseline (PNNL TAV STAP benchmark)
- Library-based code is pre-requisite for Near Memory Accelerator
 130x performance and 8,000x power efficiency gain on accelerator over C base line





Outline

Example: STAP

- Cross-call/cross library optimization with Spiral
- Library-based hardware acceleration
- Summary

T. M. Low, Q. Guo, F. Franchetti: **Optimizing Space Time Adaptive Processing Through Accelerating Memory-Bounded Operations.** IEEE High Performance Extreme Computing Conference (HPEC), 2015.



Space Time Adaptive Processing (STAP)



dense data cube





Input: 32 MB Output: 128 MB Millions of Math Ops

SWAP requirement: high performance, low power

Main Computational Stages in STAP



Many memory-bounded operations

Based on PNNL's Third-order Doppler STAP implementation (DARPA PERFECT STAP Benchmark)

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Background: FFTW 3

- Latest version of FFTW supports threading, SIMD, MPI
- De-facto standard FFT library for HPC distributed with Linux, installed everywhere
- Autotuning + program generation small hand-written core
- Interface widely supported

Intel MKL, IBM ESSL, AMD ACML,...

```
#include <fftw3.h>
. . .
   fftw_complex *in, *out;
   fftw_plan p;
   . . .
   in = (fftw complex*) fftw malloc(sizeof(fftw complex) * N);
   out = (fftw complex*) fftw malloc(sizeof(fftw complex) * N);
   p = fftw_plan_dft_1d(N, in, out, FFTW_FORWARD, FFTW_ESTIMATE);
   fftw_execute(p); /* repeat as needed */
   . . .
   fftw_destroy_plan(p);
   fftw_free(in); fftw_free(out);}
```



FFTW is a C subroutine library for computing the discrete Fourier transform (DFT) in one or more dimensions, of arbitrary input size, and of both real and complex data (as well as of even/odd data, i.e. the discrete cosine/sine transforms or DCT/DST). We believe that FFTW, which is free software, should become the FFT library of choice for most applications.

The latest official release of FFTW is version 3.3.4, available from our download page. Version 3.3 introduced support for the AVX x86 extensions, a distributed-memory implementation on top of MPI, and a Fortran 2003 API. Version 3.3.1 introduced support for the ARM Neon extensions. See the release notes for more information

The FFTW package was developed at MIT by Matteo Frigo and Steven G. Johnson

Our benchmarks, performed on on a variety of platfor other publicly available FFT software, and is even co codes, however, FFTW's performance is portable: the modification. Hence the name, "FFTW," which stand in the West "

Features

FFTW 3.3.4 is the latest official version of FFTW (re some of FFTW's more interesting features:

- · Speed. (Supports SSE/SSE2/Altivec, since vers
- · Both one-dimensional and multi-dimensional · Arbitrary-size transforms. (Sizes with small p
- for prime sizes.) · Fast transforms of purely real input or output of
- · Transforms of real even/odd data: the discrete types I-IV. (Version 3.0 or later.)
- Efficient handling of multiple, strided transfo transform one dimension of a multi-dimensional
- Parallel transforms: parallelized code for platfo or OpenMP. An MPI version for distributed-me
- · Portable to any platform with a C compiler. · Documentation in HTML and other formats.
- · Both C and Fortran interfaces.
- · Free software, released under the GNU General also be purchased from MIT, for users who do details.) (See also the FAQ.)

If you are still using FFTW 2.x, please note that FFT FFTW 3.x. The API of FFTW 3.x is incompatible w (see the FAQ or the manual)

Special Issue on: Subscribe to the fftw-announce mailing list to receive PROGRAM GENERATION, OPTIMIZATION AND PLATFORM ADAPTATION

g Our Past: Electrical Engineering Hall of Fanse: Alexander Graham Bel



Matteo Frigo and Steven G. Johnson: The Design and Implementation of FFTW3. Proceedings of the IEEE 93 (2), 216–231 (2005). Invited paper, Special Issue on Program Generation, Optimization, and Platform Adaptation.



Doppler Transform: FFT + Corner Turn



Combine loop of FFTs plus subsequent corner turn into one FFTW call

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Use FFTW Guru Interface for Data Copy

Zero pad plus batch transpose



const fftwf_iodim howmany_dims[3] =
{{n:N_RANGE, is:1, os:N_DOP},
{n:N_PULSES, is:N_RANGE, os:1},
{n:N_CHAN,
is:N_RANGE*N_PULSES,
os:N_RANGE*N_DOP}};

fftwf_execute(plan);

```
Batch transpose
```

```
const fftwf_iodim howmany_dims[3] =
{{n:N_DOP, is:1, os:N_RANGE},
{n:N_RANGE, is:N_DOP, os:1},
{n:N_CHAN,
is:N_RANGE*N_DOP,
os:N_RANGE*N_DOP}};
```

fftwf_execute(plan);

FFTW Rank-0 FFT abstracts copy, transpose, gather, scatter

Borrowing FFTW's Guru Interface for BLAS

FFTW guru interface

strong support for batch FFTs and n-dimensional data cubes

```
typedef struct{
    int n; // size of the dimension
    int is; // stride for input
    int os; // stride for output
} fftw_iodim;
```

/* FFTW Guru Interface */ fftw_plan fftw_plan_guru_dft(int rank, const fftw_iodim *dims, int howmany_rank, const fftw_iodim *howmany_dims, fftw_complex *in, fftw_complex *out, int sign, unsigned flags);

Standard BLAS interface

Fortran 77 style interface

```
void cblas_cdotc_sub (const int N, const void * x, const int incx,
const void * y, const int incy, void * dotc);
```

Generalization: BLAS guru interface

borrow FFTW's data and batch representation for BLAS operations

```
typedef struct{
    int n;
    int i0s; // stride for input0
    int i1s; // stride for input1
} blas_indim;
// (rank, dims[rank]) describes the basic BLAS operation size
    int rank,
    blas_indim *dims,
// (howmany_rank, howmany_dims[rank]) describes the "vector" size
    int howmany_rank,
    blas indim *howmany dims);
```

Use BLAS guru interface in backend but do not expose to end user

Use OpenMP to Avoid Changing BLAS Interface

- Absolutely cannot change BLAS set-in-stone standard since 1979
- Supported by everybody MKL, ESSL, ACML, CUBLAS,...
- Idea: Use OpenMP to express batch mark loops as independent
- Use compiler to extract batch BLAS descriptor automatically translate BLAS + OpenMP to BLAS Guru Interface





After Transformation: STAP = 4 Library Calls



Result: STAP is expressed using four library calls + OpenMP directives



Outline

- Example: STAP
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DSL Compiler for Global Transformations

- Parse library calls and OpenMP convert to Spiral's operator language (OL)
- Spiral performs global optimizations kernel merging, data layout transformations,...
- Output CPU or accelerator code run with Intel MKLK or our own accelerator
- Utilize BLAS Guru interface

our accelerator implements BLAS Guru



M. Püschel, J. Moura, J. Johnson, D. Padua, M. Veloso, B. Singer, J. Xiong, F. Franchetti, A. Gacic, Y. Voronenko, K. Chen, R. W. Johnson, N. Rizzolo, **"SPIRAL: Code Generation for DSP Transforms,"** Proceedings of the IEEE *Special Issue on Program Generation, Optimization, and Adaptation*, 2005

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Spiral Approach

What is Spiral?

Traditionally



Platform-Aware Formal Program Synthesis

Model: common abstraction = spaces of matching formulas



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Operators

Definition

- Operator: Multiple complex vectors \rightarrow multiple complex vectors
- Higher-dimensional data is linearized
- Operators are potentially nonlinear

$$\mathsf{M}: \begin{cases} \mathbb{C}^{n_0} \times \cdots \times \mathbb{C}^{n_{k-1}} \to \mathbb{C}^{N_0} \times \cdots \times \mathbb{C}^{N_{\ell-1}} \\ (\mathbf{x}_0, \mathbf{x}_1, \dots, \mathbf{x}_{k-1}) \mapsto \mathsf{M}(\mathbf{x}_0, \mathbf{x}_1, \dots, \mathbf{x}_{k-1}) \end{cases}$$

Example: Matrix-matrix-multiplication (MMM)



Key to capture FFTs, numerical linear algebra, message passing in one framework

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Operator Language

name

definition

Linear, arity (1,1)identity vector flip transposition of an $m \times n$ matrix matrix $M \in \mathbb{C}^{m \times n}$ Multilinear, arity (2,1) Point-wise product Scalar product Kronecker product Others Fork Split Concatenate Duplication Min Max

| $I_n: \mathbb{C}^n \to \mathbb{C}^n; \mathbf{x} \mapsto \mathbf{x}$ |
|--|
| $J_n: \mathbb{C}^n \to \mathbb{C}^n; \ (x_i) \mapsto (x_{n-i})$ |
| $L_m^{mn}: \mathbb{C}^{mn} \to \mathbb{C}^{mn}; \mathbf{A} \mapsto \mathbf{A}^T$ |
| $\mathbf{M}: \mathbb{C}^n \to \mathbb{C}^m; \mathbf{x} \mapsto M\mathbf{x}$ |

$$P_n: \mathbb{C}^n \times \mathbb{C}^n \to \mathbb{C}^n; ((x_i), (y_i)) \mapsto (x_i y_i)$$

$$S_n: \mathbb{C}^n \times \mathbb{C}^n \to \mathbb{C}; ((x_i), (y_i)) \mapsto \Sigma(x_i y_i)$$

$$K_{m \times n}: \mathbb{C}^m \times \mathbb{C}^n \to \mathbb{C}^{mn}; ((x_i), \mathbf{y})) \mapsto (x_i \mathbf{y})$$

Fork_n: $\mathbb{C}^n \to \mathbb{C}^n \times \mathbb{C}^n$; $\mathbf{x} \mapsto (\mathbf{x}, \mathbf{x})$ Split_n: $\mathbb{C}^n \to \mathbb{C}^{n/2} \times \mathbb{C}^{n/2}$; $\mathbf{x} \mapsto (\mathbf{x}^U, \mathbf{x}^L)$ $\oplus_n : \mathbb{C}^n \times \mathbb{C}^m \to \mathbb{C}^{n+m}$; $(\mathbf{x}, \mathbf{y}) \mapsto \mathbf{x} \oplus \mathbf{y}$ dup_n^m: $\mathbb{C}^n \to \mathbb{C}^{nm}$; $(\mathbf{x} \mapsto \mathbf{x} \otimes I_m$ min_n: $\mathbb{C}^n \times \mathbb{C}^n \to \mathbb{C}^n$; $(\mathbf{x}, \mathbf{y}) \mapsto (\min(x_i, y_i))$ max_n: $\mathbb{C}^n \times \mathbb{C}^n \to \mathbb{C}^n$; $(\mathbf{x}, \mathbf{y}) \mapsto (\max(x_i, y_i))$

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Some Application Domains in OL

Linear Transforms

Software Defined Radio



Matrix-Matrix Multiplication

Synthetic Aperture Radar (SAR)

Formal Approach for all Types of Parallelism

- Multithreading (Multicore)
- Vector SIMD (SSE, VMX/Altivec,...)
- Message Passing (Clusters, MPP)
- Streaming/multibuffering (Cell)
- Graphics Processors (GPUs)
- Gate-level parallelism (FPGA)
- HW/SW partitioning (CPU + FPGA)

$$\begin{split} \mathbf{I}_{p} \otimes_{\parallel} A_{\mu n}, \quad \mathbf{L}_{m}^{mn} \bar{\otimes} \mathbf{I}_{\mu} \\ A \bar{\otimes} \mathbf{I}_{\nu} \quad \underbrace{\mathbf{L}_{2}^{2\nu}}_{\mathrm{isa}}, \quad \underbrace{\mathbf{L}_{\nu}^{2\nu}}_{\mathrm{isa}}, \quad \underbrace{\mathbf{L}_{\nu}^{\nu^{2}}}_{\mathrm{isa}} \\ \mathbf{I}_{p} \otimes_{\parallel} A_{n}, \quad \underbrace{\mathbf{L}_{p}^{p^{2}} \bar{\otimes} \mathbf{I}_{n/p^{2}}}_{\mathrm{all-to-all}} \\ \mathbf{I}_{n} \otimes_{2} A_{\mu n}, \quad \mathbf{L}_{m}^{mn} \bar{\otimes} \mathbf{I}_{\mu} \\ \prod_{i=0}^{n-1} A_{i}, \quad A_{n} \bar{\otimes} \mathbf{I}_{w}, \quad P_{n} \otimes Q_{w} \\ \prod_{i=0}^{n-1} A_{i}, \quad \mathbf{I}_{s} \bar{\otimes} A, \quad \underbrace{\mathbf{L}_{n}^{m}}_{\mathrm{bram}} \\ \underbrace{A_{1}}_{i=0}, \quad \underbrace{A_{2}}_{i}, \quad \underbrace{A_{3}}_{j}, \quad \underbrace{A_{4}}_{j} \\ \underbrace{A_{1}}_{j}, \quad \underbrace{A_{2}}_{j}, \quad \underbrace{A_{3}}_{j}, \quad \underbrace{A_{4}}_{j} \\ \end{split}$$

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Autotuning in Constraint Solution Space

Translating an OL Expression Into Code

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STAP in SPIRAL's OL specification

 $(I_D \otimes I_B \otimes (I_V \otimes I_S \otimes (Dot \circ Extract)) \circ (I_V \otimes \frac{1}{|| Dot^{CF} ||_{\lambda}})) \circ$ Inner Products

 $(I_D \otimes I_B \otimes I_V \otimes (Trsv_{bwd}^{CF} \circ Trsv_{fwd}^{CF})) \circ$

 $(I_{\mathcal{D}} \otimes I_{\mathcal{D}} \otimes Chol^{CF}) \circ$

Linear System Solver

| $(I_B \otimes I_D \otimes (\frac{1}{S} \times (I_S \otimes (Her^{CF} \circ Extract))))) \circ$ | Covariance Estimate |
|--|----------------------------|
| $(I_C \otimes L_R^{RD}) \circ$ | FFT + Corner Turn |
| $I_{C}(\mathbf{X}) I_{D}(\mathbf{X}) D\Gamma I_{D}$ | |

STAP: Necessary Optimization

Problem: BLAS/LAPACK interface

Merged Operation

Batched Operation

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STAP: SPIRAL Optimization

BLAS2 to BLAS3 call

Interpreting the OL Specification

After SPIRAL's transformations

Loop coalescing

OL vs. FFTW Guru Inteface

FFTW guru-interface

Batched descriptor for FFT computation

fftwf_plan_guru_dft(

OL representation of FFTW guru interface

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Optimizing STAP with Spiral

- Input: C program with BLAS and FFTW calls
- Spiral Input: STAP C program only using FFTW and BLAS guru calls
- This is equivalent to a OL formula in Spiral
- Enables full-program data layout optimization and kernel merging
- Final program: efficient on CPU, Accelerator can target novel accelerators infrastructure

This paves the way for our 3DIC memory side accelerator (discussed next)

Outline

- Example: STAP
- Cross-call/cross library optimization with Spiral
- Library-based hardware acceleration
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Q. Guo, T.-M. Low, N. Alachiotis, B. Akin, L. Pileggi, J. C. Hoe, and F. Franchetti: **Enabling Portable Energy Efficiency with Memory Accelerated Library.** IEEE/ACM MICRO-48, 2015, *to appear*.

Overview: Memory-Side Accelerators

Accelerator behind DRAM interface

- No off-DIMM data traffic and SERDES
- Huge problem sizes possible
- 3D stacking is enabling technology

Configurable array of accelerators

- Domain specific, highly configurable
- Cover DoD-relevant kernels

System CPU

Standard: Multicore CPU+GPU

Software stack

- User level: standard numeric libraries
 BLAS1/2, FFTW, SpMV/SpGEMM,...
- OS, driver, compiler, runtime system support necessary for drop-in replacement

Accelerator Hardware Architecture

Accelerator tiles

- One accelerator tile per 3D-DRAM vault
- Can be linked to one big accelerator
- Configurable/programmable: units, interconnect, iterators

Programming model

- Memory mapped device
- Physical memory addressing
- Data and command segment in DRAM
- Controlled via read/writes to command addresses

Accelerator Software Architecture

Accelerator software abstraction

- memory mapped device
- command and data address space
- kernel/virtual memory configuration

Low level user API

- device driver interface
- Iow level C configuration library

Application level API

- transparent device-aware malloc/free
- standard low intensity math libraries: BLAS-1, BLAS-2, FFTW, sparse mat/vec, copy/reshape, corner turn
- "guru" math library interfaces
- OpenACC directives + proto compiler

```
// TAV STAP example
11
// kernel reimplemented with BLAS and OpenACC
11
float *adaptive weights;
float *steering_vectors;
#pragma declare \
    device_resident(adaptive_weights);
#pragma declare \
    device_resident(steering_vectors);
adaptive_weights = XMALLOC(sizeof(complex)*
    num adaptive weight elements);
steering_vectors = XMALLOC(sizeof(complex)*
    num_steering_vector_elements);
#pragma acc data copyin(adaptive_weights, \
    steering_vectors), copyout(accums)
#pragma acc kernels loop
for (sv = 0; sv < N STEERING; ++sv)
  for (block = 0; block < N_DOP*N_BLOCKS; ++block)</pre>
    accum.re = accum.im = 0.0f;
    cblas cdotc sub(TDOF*N CHAN,
       (float*)adaptive_weights[block][sv],
       1,
       (float*)steering_vectors[sv],
       1,
       (float*)&accums[block][sv]);
 }
. . .
```


Hardware in the Loop Simulation

Accelerator Simulation

- Timing: Synopsis DesignWare
- Power: DRAMSim2, Cacti, Cacti-3DD, McPAT

Full System Evaluation

- Run code on real system (Haswell, Xeon Phi) or in simulator (SimpleScalar,...)
- Normal DRAM access for CPU, but trap accelerator command memory space, invoke simulator

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Accelerating the TAV STAP Benchmark

STAP structure: 4 phases

- Doppler: batch FFT
- Covariance estimation: outer product
- System solver: Cholesky or QR
- Adaptive weighting: inner product

STAP memory-side acceleration

- On CPU: BLAS-3/Cholesky
- On accelerator: FFT, BLAS-1, BLAS-2

Software interface

- Drop-in replacement for Intel MKL: FFTW, BLAS-1/2/3
- OpenACC pragmas for batch BLAS-1/2

No DMA/copy-in/copy-out necessary for accelerator

STAP Performance Results

Speedup (Times)

STAP Power Efficiency Results

GFLOPS/W Gain over Baseline (TAV)

EDP Reduction (Times)

Memory Layout Accelerator

Data Reshape Unit (DRU)

B. Akin, F. Franchetti, J. C. Hoe: Data Reorganization in Memory Using 3D-stacked DRAM, 42nd International Symposium on Computer Architecture (ISCA), 2015.

Intel MKL (Math Kernel Library) functions:

To I/O links

mkl_simatcopy (const char ordering, char trans, size_t rows, size_t cols, const float alpha, float * AB, size_t lda, size_t ldb); mkl_somatcopy (char ordering, char trans, size t rows, size t cols, const float alpha, float * A, size_t lda, float * B, size_t ldb); void **pstrmr2d** (char *uplo, char *diag, MKL INT *m, MKL INT *n, float *a, , ..., MKL INT *jb , MKL INT *descb , MKL INT*ictxt); // ScaLAPACK void cblas_scopy (const MKL INT n, const float *x, const MKL INT incx, ...); void **cblas sswap** (const MKL INT *n*, float **x*, const MKL INT *incx*, float **y*,...); pslared2d (n, ia, ja, desc, byrow, byall, work, lwork) **pslaswp** (direc, rowcol, n, a, ia, ja, desca, k1, k2, ipiv)

Accelerating MKL Reorganization Routines

CPU (i7-4770K)

📕 GPU (GTX 780) 🛛 📕

DRU (MH)

Reshape Throughput [GB/s]

Energy Efficiency [GB/J]

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Summary

Target: dense scientific and HPEC kernels math heavy, regular, good library coverage

HPC Library + OpenMP + C as DSL
 View program as specification

Enormous efficiency gains are possible
 Novel accelerators + Spiral optimization

Users' Guide Prof Cetter A chemical Adv. (Factor Chemical Content) A chemical Adv. (Factor Chemical Content)

