Power Performance Reliability Co-Design: 3D IC Case Study

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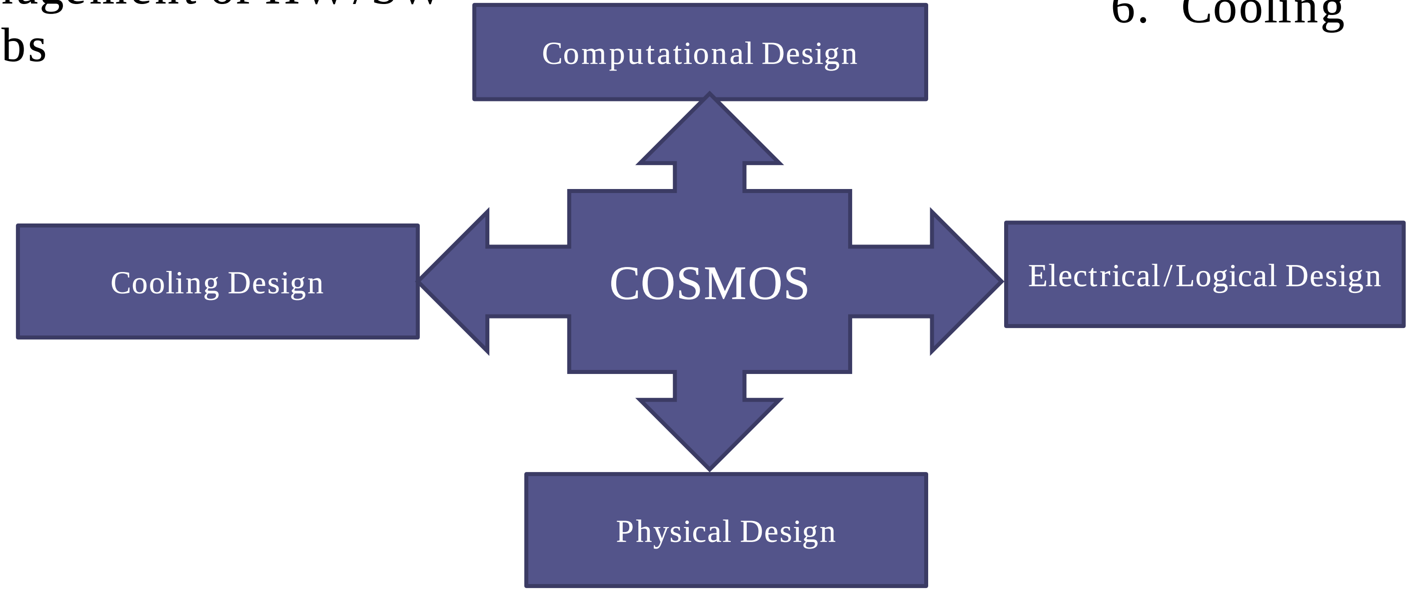
Overarching Agenda: Co-Simulation and Co-Modeling Driven Co-Design of Computing Systems

Runtime CoDesign

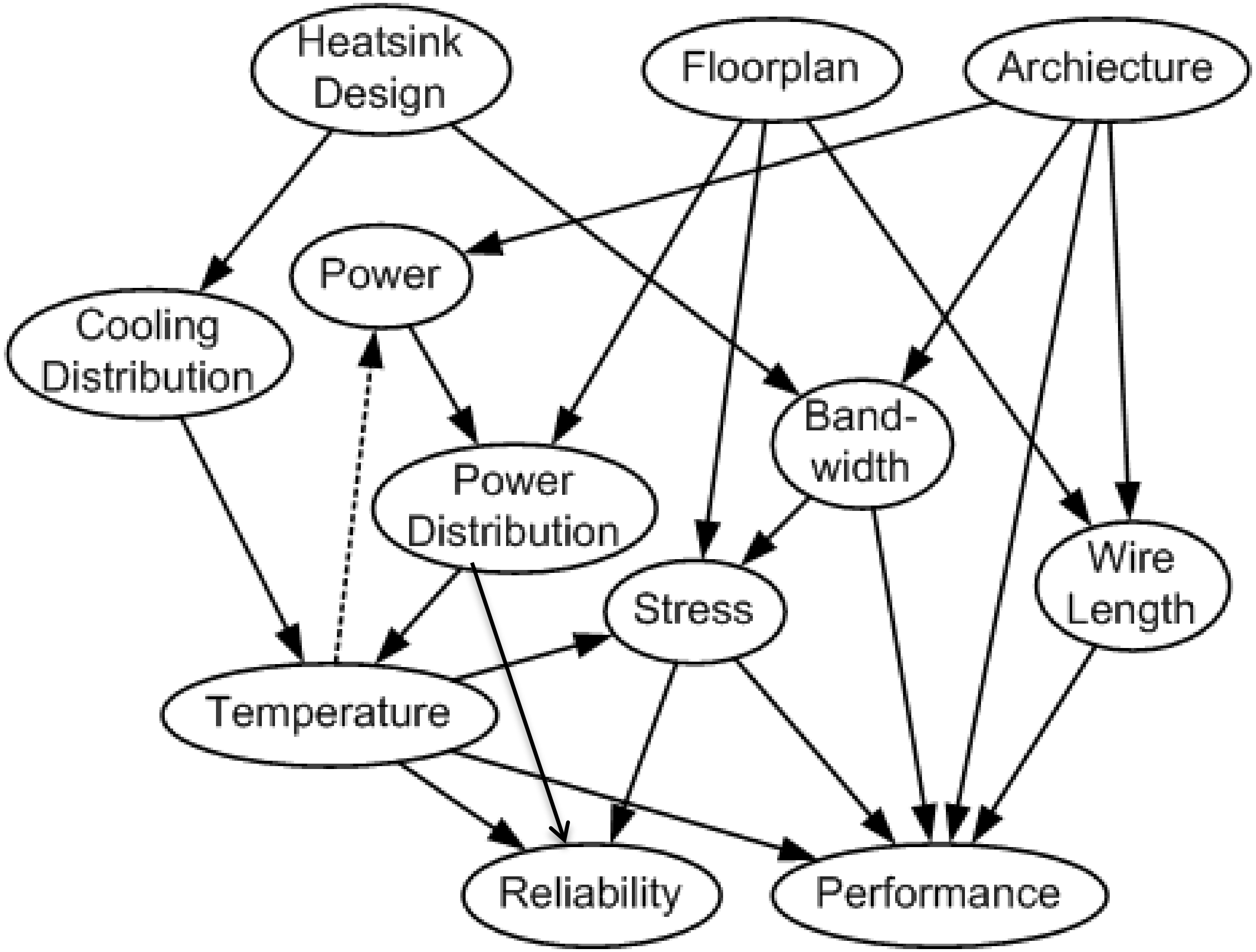
1. Online model building from chip/board level sensors
2. Feedback control based management of HW/SW knobs

Design Time CoDesign

1. Application
2. Architecture
3. System
4. Devices
5. Packaging
6. Cooling



How do we do Co-Design?
(weighted?) Co-Design Graph (Sub-Application Level)



3D ICs

System Throughput

- 3D eliminates low-bandwidth off-chip links that stall benefits of processor throughput
- Enables high-throughput architectures

System Power

- Reduces system capacitance, losses, and power in signaling: on-chip wires=50-70% total chip capacitanc

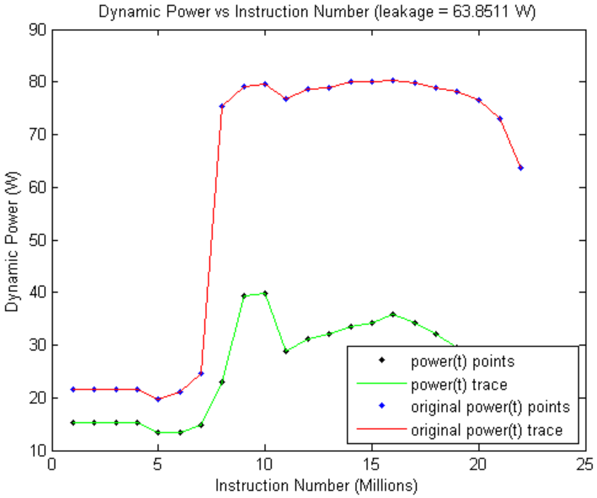
Today's off-chip links:	10-35 mW/Gbps
3D:	<1 mW/Gbps

Heterogeneous Integration

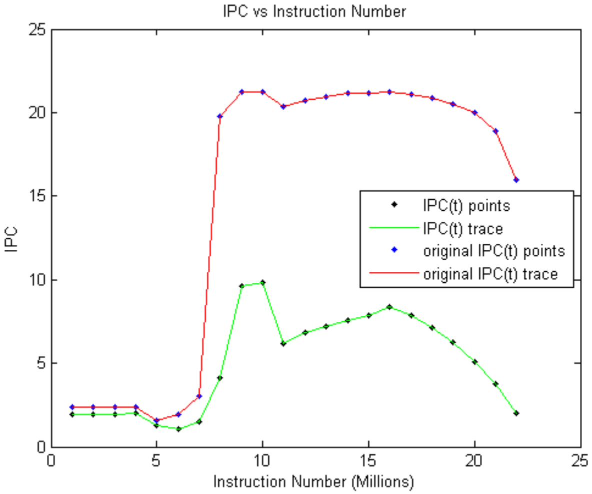
- Provide monolithic like performance for photonics, MEMS, sensors, non-volatile memory, etc with CMOS

System Form-factor, Cost, Yield, and Density

- Reduce chip size, which improves yield and cost
- Provides a new way to increase device density



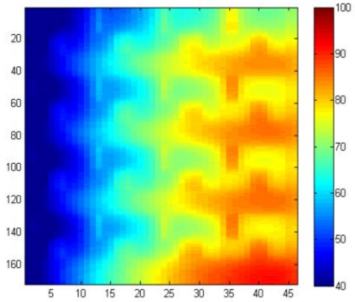
Dynamic Power vs Instruction Number (leakage = 63.8511 W)



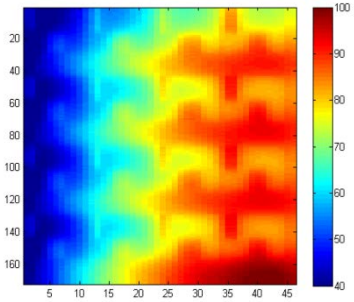
IPC vs Instruction Number

3D IC Thermal & Reliability Challenge

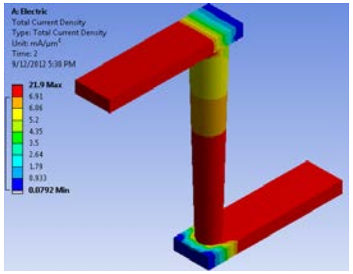
1. Sizable increase in the number of power dissipating devices. Typical logic over logic 3D IC solutions could dissipate > 300W of power. [Bar-Cohen et. al. IEEE Proc 2006]
2. Overlapped hotspots
3. Higher thermal resistance to the heat sink due to increased number of layers
4. Susceptible to new types of reliability failure mechanisms in TSVs.
    1. Electromigration
    2. Thermal Cycling and Stress Induced Cracks



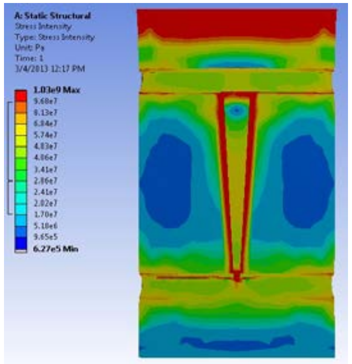
Bottom Layer



Top Layer

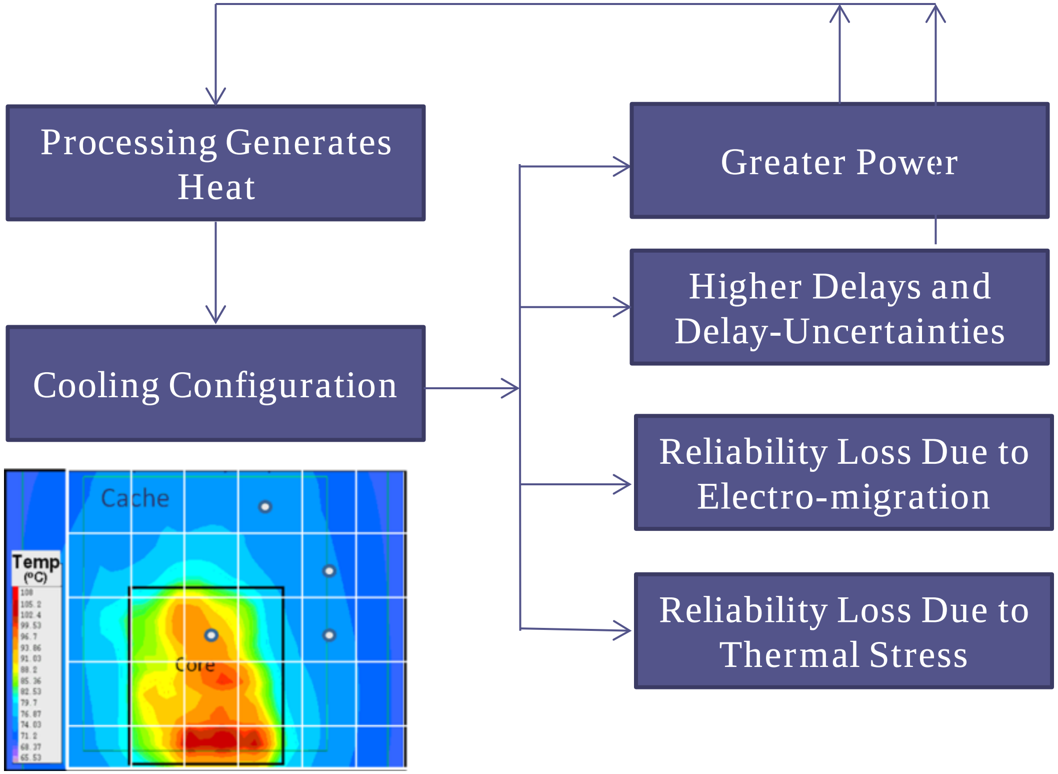


TSV Current Density



TSV Stress Profile

PPR Co-Simulation and Co-Modeling



Processing Generates Heat

Cooling Configuration

Greater Power

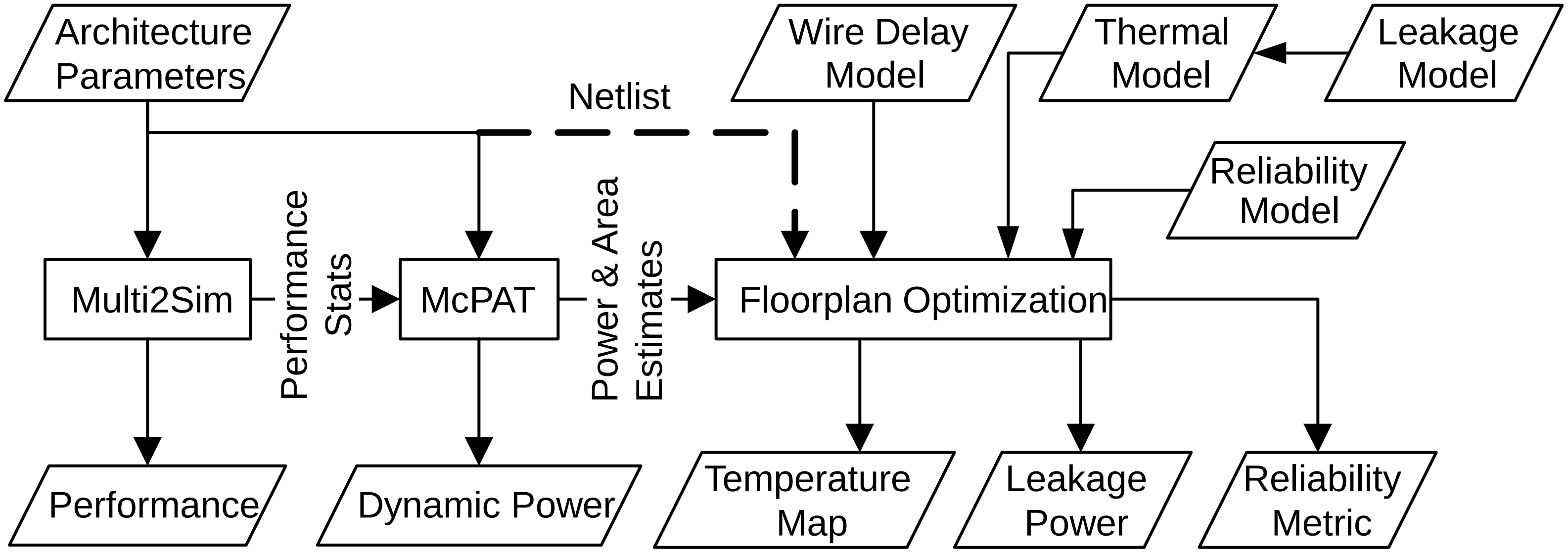
Higher Delays and Delay-Uncertainties

Reliability Loss Due to Electro-migration

Reliability Loss Due to Thermal Stress

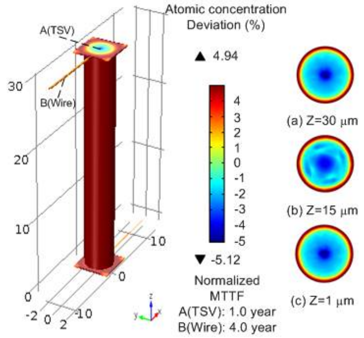
- Conventional cooling approaches follow a post-fix method.
- The electrical, thermal, fluidic and mechanical aspects of the system are interdependent.
  - Postfix based design of the fluidic/cooling aspect of the system undermines this interdependence and misses opportunities for optimization

Design Space Simulation Environment



- Given a 3D CPU architectural solution space:
  - num cores = {16, 32, 64}
  - num MC = num_cores/{8, 4, 2}
  - clock frequency = {2.4, 3.0, 3.6} GHz
- We identify the architecture with the highest performance subject to:
  - Timing/wirelength constraint: (slack > 0)
  - Thermal constraint (temp < 85 C)
  - Reliability Constraint (reliability > 99%)

Statistical Reliability Model for TSV

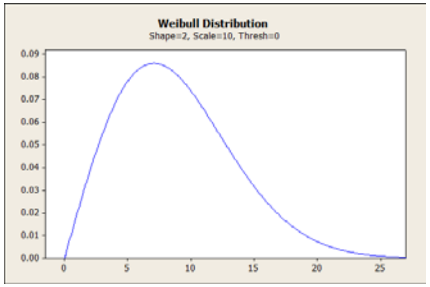


$$\frac{\partial c}{\partial t} + \nabla \cdot \vec{q} = 0$$

$$\vec{q} = -D\nabla c + \frac{Dc\vec{j}e\rho Z}{kT} + \frac{Dc\Omega}{kT} \cdot (\nabla \sigma_m) + \frac{DcQ^*}{kT} \cdot \frac{\nabla(T)}{T}$$

c: Atomic concentration
$\vec{j}$: Current density
T: Temperature

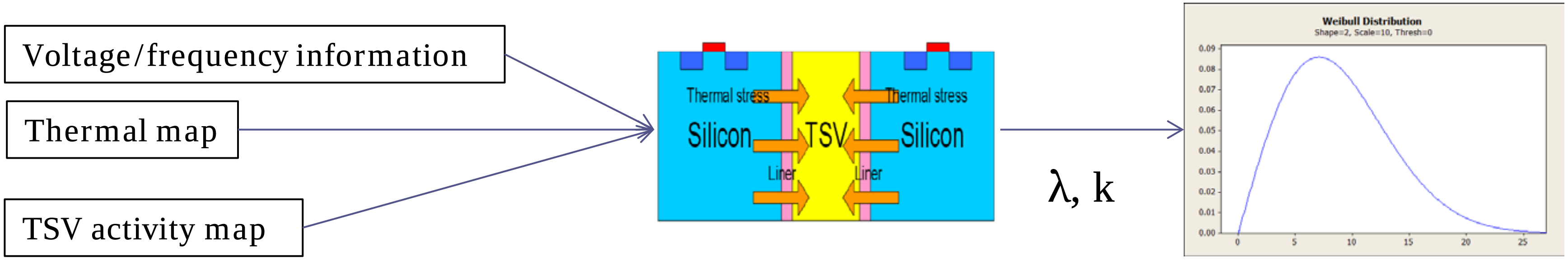
σ: Thermal stress
Others: constants



Each Weibull distribution is determined by a shape parameter k (assumed to be a constant) and a scale parameter λ.

$$\lambda \propto MTTF_{EM} \propto \left(J_{avg}\right)^{-2} e^{\frac{E_a}{kT}}$$

J_{avg} is the equivalent DC current of an AC signal, which depends on voltage, frequency, and TSV activity.

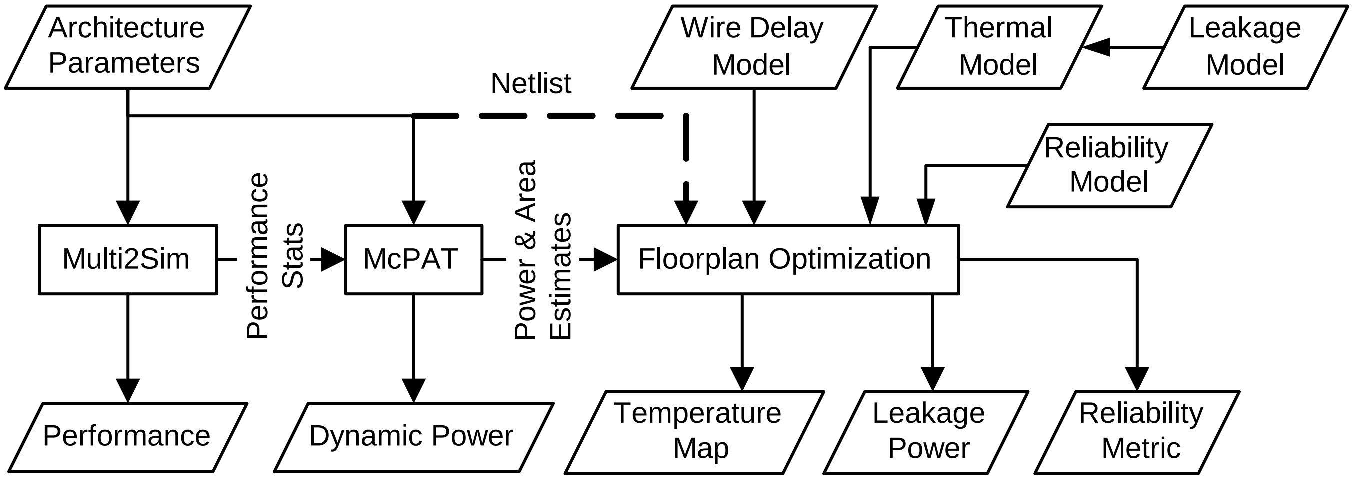

Voltage/frequency information

Thermal map

TSV activity map

λ, k

Statistical Reliability Model



Architecture Parameters

Netlist

Wire Delay Model

Thermal Model

Leakage Model

Reliability Model

Multi2Sim

Performance Stats

McPAT

Power & Area Estimates

Floorplan Optimization

Performance

Dynamic Power

Temperature Map

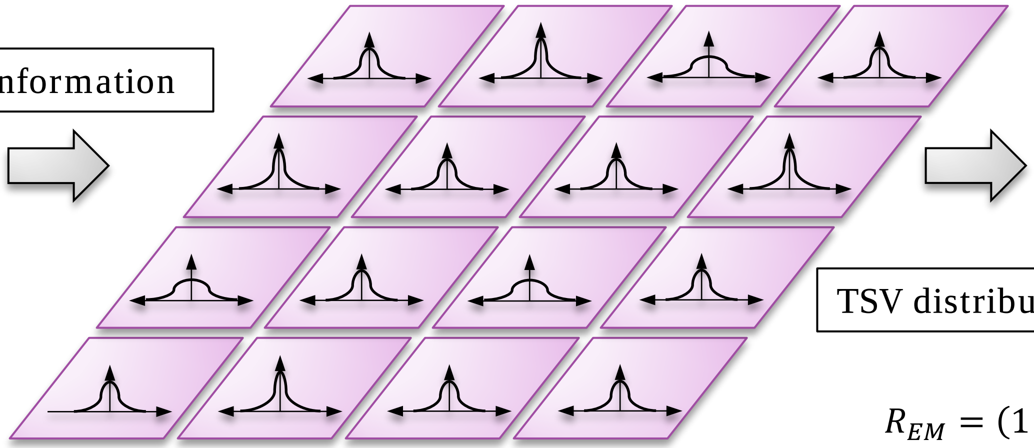
Leakage Power

Reliability Metric

Voltage/frequency information

Thermal map

TSV activity map



Grid-level TSV failure PDF

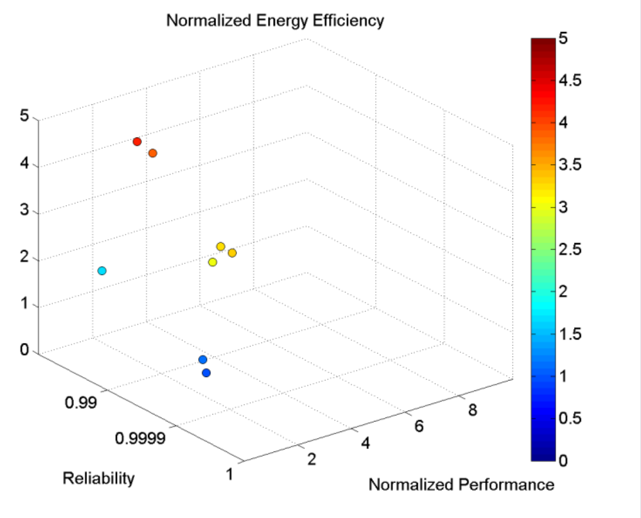
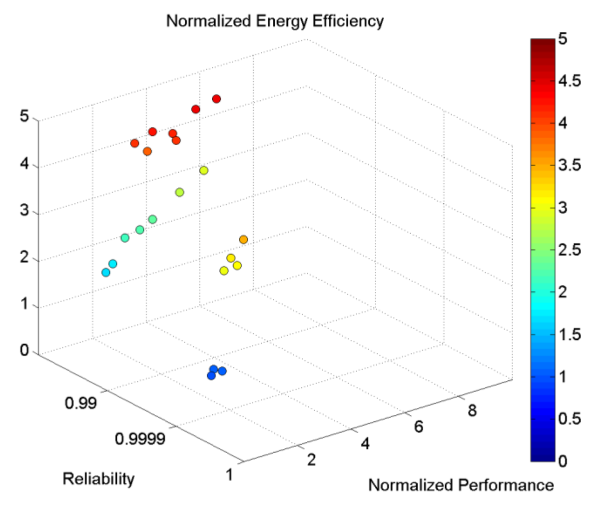
TSV distribution

System-level reliability estimation

$$R_{EM} = (1 - P_{EM}) = \prod_{i \in TSV} (1 - P_{EM}^{i})$$

P^{i}_{EM} = Prob of i-th TSV failing in 3 years

Scatter Plots of Thermally Feasible Architectures

	Air Cooled	**MF Cooled**
		

Air Cooled Reliability Unaware (99% Reliability Constraint)

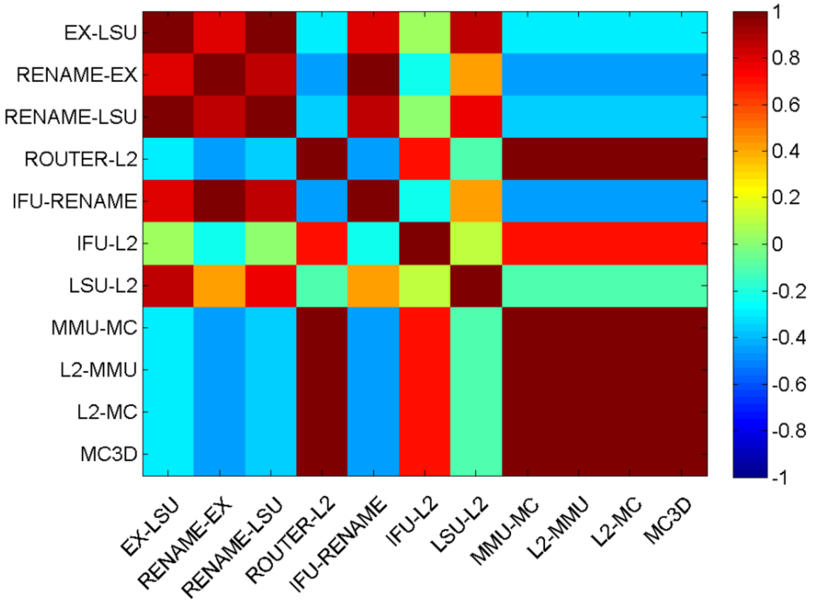
	#cores	#MC	Freq	Power	MaxT	IPnS	Energy Efficiency
barnes	16	8	3.6	110	74.5	36.9	12.4
blackscholes	16	8	3.6	102	78.5	27.1	7.2
bodytrack	16	8	3.6	110	74.4	35.9	11.7
dedup	16	8	3.6	109	75.5	27.9	7.1
fft	16	8	3.6	115	75.5	32.3	9.1
fluidanimate	16	8	3.6	133	77.0	46.1	16.0
ocean	32	16	3.0	172	78.8	15.0	1.3
radix	16	8	3.6	113	75.1	38.5	13.1
swaptions	16	8	3.6	118	75.5	44.1	16.5
water-nsquared	16	8	3.6	147	81.7	72.6	35.9
water-spatial	16	4	3.0	106	83.4	80.1	60.4
avg	**1.00x**	**1.00x**	**1.00x**	**1.00x**	**1.00x**	**1.00x**	**1.00x**

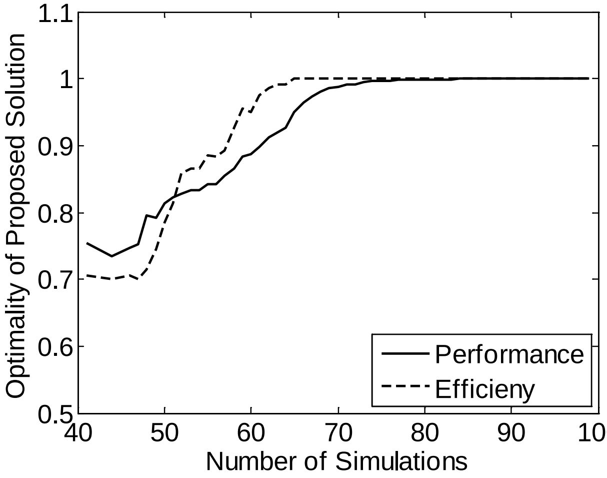
MF Cooled Reliability Aware (99% Reliability Constraint)

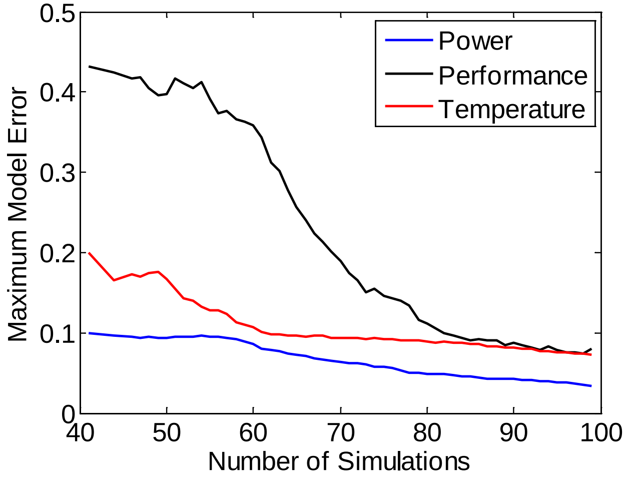
	#cores	#MC	Freq	Power	MaxT	IPnS	Energy Efficiency
barnes	64	16	3.6	376	84	103.1	28.3
blackscholes	64	8	3.6	258	72	50.2	9.8
bodytrack	64	16	3.6	337	79	53.8	8.6
dedup	32	16	3.6	246	66	52.0	11.0
fft	32	16	3.6	255	67	59.6	13.9
fluidanimate	32	16	3.6	277	71	84.6	25.8
ocean	32	16	3.6	209	62	17.6	1.5
radix	64	16	3.6	347	80	49.4	7.1
swaptions	32	16	3.6	253	68	76.7	23.2
water-nsquared	32	16	3.6	297	73	122.6	50.6
water-spatial	64	8	3.0	300	71	187.5	117.1
avg	**2.57x**	**1.76x**	**1.02x**	**2.36x**	**0.93x**	**1.76x**	**1.32x**

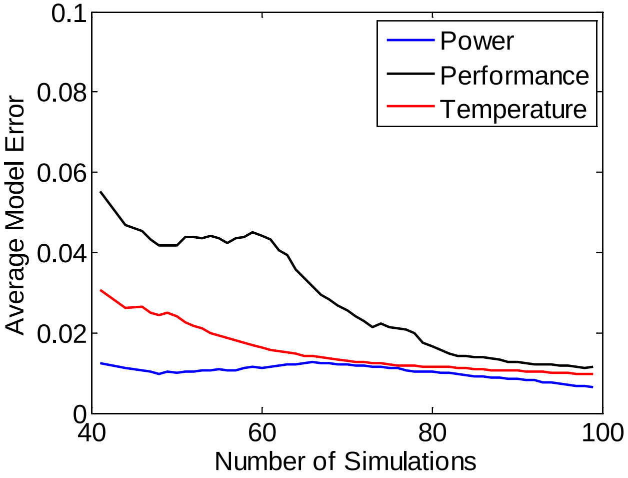
On-Going Work

1. The TSV reliability model is purely statistical. Refinements driven from multiphysics.
2. Other Reliability Loss Models (PG Noise, Stress etc.)
3. Correlations in signal activity imply correlations in reliability degradation.
4. Architectural parameters are still exhaustively searched.
    1. Need an adaptive model building based approach where the arch. solution space is modeled by fitting the data from a few simulations. The model is used to predict the optimal solution.
    2. Preliminary data illustrated below.









Acknowledgements

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